

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S59	1270	(delay with adjust\$3) and hierarch\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:08
S60	838	synchroniz\$5 and S59	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:10
S61	81	(wir\$3 near4 length) and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:10
S62	72	point and S61	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/22 16:13
S63	4	((point or terminal) with (equal or equaliz\$3 or uniform\$3) with length) and S61	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 11:44

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	630	clock adj input adj circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:04
L7	13	(hierarch\$4 near3 block) and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 11:47
L8	54	(clock adj input adj circuit) with (synchronous\$2 or synchronized)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:02
L9	2	(hierarch\$4 near3 block) and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 11:48
L10	10	hierarch\$4 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:03
L11	56	(clock adj input adj circuit) with (synchronous\$2 or synchroniz\$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:02
L12	64	(clock adj input adj circuit) with (synchronous\$2 or synchroniz\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:05
L13	12	hierarch\$4 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:12
L14	5	length and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:03
L15	2361	clock near input near circuit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:07
L16	199	(clock near input near circuit) with (synchronous\$2 or synchroniz\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:05

## EAST Search History

L17	14	hierarch\$4 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:08
L18	5	length and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:06
L19	195	(clock near input near circuit).clm.	US-PGPUB	OR	ON	2006/08/23 12:07
L20	29	((clock near input near circuit) same (synchronous\$2 or synchroniz\$3)).clm.	US-PGPUB	OR	ON	2006/08/23 12:08
L21	3	hierarch\$4 and 20	US-PGPUB	OR	ON	2006/08/23 12:09
L23	2	length.clm. and 21	US-PGPUB	OR	ON	2006/08/23 12:10
L24	2398	716/4.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:42
L25	2	("5849610").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2006/08/23 12:15
L26	0	hierarch\$4 and 25	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:15
L27	1776	716/5.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:58
L28	1472	716/6.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/08/23 12:58